REMARKS

The indication of allowable subject matter in claims 7 and 8 is acknowledged and appreciated. Accordingly, claim 7 has been rewritten into independent form to include the limitations of the underlying claims.

Claims 1, 3-5, 7, 8 and 10 are objected to for minor informalities. In order to expedite prosecution and improve grammar/syntax, the claims have been amended as suggested by the Examiner except for the requested change of "operation simulation" throughout the claims to --simulation operation--. It is respectfully submitted that the claim language as currently written is correct in that it defines a "circuit operation simulation"; i.e., a "simulation" of a circuit operation. In other words, "circuit operation" or "operation" is the "thing" being simulated. On the other hand, the phrase "circuit simulation operation" as suggested by the Examiner could imply an "operation" of a circuit simulation which is grammatically/technically confusing. Based on the foregoing, it is respectfully requested that the objection to the claims be withdrawn.

Claims 7 and 8 stand rejected under 35 U.S.C. § 112, second paragraph. This rejection is respectfully traversed for the following reasons. The Examiner alleges that the recitation of "circuit hierarchical information" renders the claims indefinite because "there is no prior recitation that the semiconductor circuit is hierarchical." However, it is respectfully submitted that the recitation "circuit hierarchical information" ***itself*** introduces the feature that the circuit has hierarchical information. Indeed, both claims 7 and 8 recite in pertinent part, "wherein a low-precision, high-speed operation simulation is executed ... ***to prepare*** ... circuit hierarchical information on the semiconductor circuit" (emphasis added) as the ***first*** occurrence of such a limitation. It should be noted that the aforementioned first occurrence of the circuit hierarchical

information is not functionally/structurally defined, but rather, is being ***prepared*** as a way to first introduce the limitation. It can thereafter be operationally used so that its initial preparation does not lead to any structural/functional gap among the claims. In this regard, it is respectfully submitted that any additional recitation that the semiconductor circuit includes hierarchical information would be unnecessarily redundant and confusing.

Based on the foregoing, it is submitted that claims 7 and 8 are definite. Accordingly, it is respectfully requested that the rejection of claims 7 and 8 under 35 U.S.C. § 112, second paragraph be withdrawn.

Claims 1 and 9-11 are independent and stand rejected under either § 102 or 103 over Applicants' admitted prior art ("APA") as disclosed in JP '578 and Tani '409 ("Tani"), or a combination thereof. These rejections are respectfully traversed for the following reasons.

Conventionally, condition verification is performed after ***all*** simulations are performed (*see, e.g.,* Figure 11 of Applicants' drawings related to APA). However, because a large quantity of analytical data is required for such a conventional method, either a large quantity of analytical data is used or the condition verification process is performed multiple times. On the other hand, according to an aspect of the present invention, voltages applied to input terminals of respective circuit elements of the semiconductor circuit to be verified and currents flowing through nodes thereof can be verified to determine if they satisfy the electrical or time specifications; and a position violating the specifications, if any, can be detected while executing the operation simulation (*see, e.g.,* page 20, lines 13-22 of Applicants' specification). In other words, a simulation can be performed for a specific time and upon completion of said simulation, but not necessarily all simulations, the simulation result in the specific time can be verified. Thereafter,

the specific time can be incrementally increased and the next simulation can be performed at a subsequent time. Accordingly, in one aspect of the present invention, the specific time can be incrementally increased while repeatedly performing a simulation for a specific time and verifying the simulation result.

Referring to Fig. 2 of Applicants' drawings, for example, one exemplary embodiment of the present invention relates to a verification method (and a circuit for performing the same) wherein: (1) the simulating operation is performed with respect to time at a plurality of specific times, which are incrementally increasing, (2) the results of the simulating step are stored in memory after each simulating operation, and (3) the verification process is performed after each simulating operation (i.e., at each of the plurality of specific times).

Thus, in accordance with an aspect of the present invention, after each of a plurality of simulating operation steps of the semiconductor circuit, which are performed with respect to time, the results of the simulating operation are stored, and it is determined whether or not the circuit elements satisfy voltage and/or current specifications. As a result of the foregoing process, the method of the present invention enables high-speed operation of the verification step, which determines whether or not the circuit elements being verified satisfy the loaded condition requirements. Moreover, the present invention can eliminate the requirement of having sufficient memory (e.g., a hard disk drive) for storing the results/data of the entire operation simulation, which is required when performing the verifying step subsequent to the simulation operation step as done in the prior art. Thus, the present invention allows for the foregoing testing utilizing a relatively inexpensive computation system.

Turning to the cited prior art, both APA and Tani are completely silent as to performing a simulation for a specific time where the simulation result is verified and thereafter incrementally

increasing the specific time to perform a subsequent simulation. Indeed, the verification disclosed by Tani is basically a verification of ***static*** circuit delay information (such as fixed values of circuit operation delay times and fixed values of the signal propagating delay times due to resistances and capacitances of the interconnects), and NOT a verification performed ***dynamically*** with respect to each specific time as can be done by the present invention.

Further, the incremental delay ΔT disclosed in Tani is merely the difference between the delay time without factoring in the decrease in voltage and the delay time with the decrease in voltage being factored in (*see* col. 13, lines 19-27), but is NOT related to the verification and simulation while incrementally increasing the specification time.

Moreover, it is again respectfully submitted that Tani appears to be merely cumulative to the prior art disclosed in the background section of Applicants' specification, wherein the circuit simulation is performed first and all results are stored in a large-capacity memory device, such as a hard disk, which operates at a low speed, and thereafter (i.e., once the circuit simulation is complete) the loaded condition verification task is performed using the data stored in the large-capacity memory device.

For example, referring to Fig. 12 of Tani, this flowchart indicates that the verification step is performed as a single step after the entire simulation process is completed. Indeed, none of the various flowcharts of Tani appear to disclose that multiple simulating operations are performed with respect to time, or that a verification step is performed after each simulating operation.

As such, it is respectfully submitted that Tani does not disclose performing multiple simulating operations at a plurality of distinct times, which are incrementally increasing, and

verifying the circuit elements satisfy the predefined requirements after each simulating operation. In this regard, at best, Tani is merely cumulative to APA.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that APA does not anticipate the independent claims, nor any claim dependent thereon.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejections do not "establish *prima facie* obviousness of [the] claimed invention" as recited in the independent claims because the proposed combinations, even assuming *arguendo* they are proper, fail the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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